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WET PROCESSING:

CLEANING, ETCHING, and LIFTOFF

In this chapter we describe a variety of wet processes in which wafers are immersed in liquid reagents to achieve some beneficial fabrication effect. These include: a) wafer cleaning procedures; b) wet etching techniques; and c) *lift-off*, a patterning process wherein material is *additively deposited* on the desired locations of a wafer surface. We also introduce terminology associated with patterning technology, information applicable to the subjects covered in this chapter as well as to Chap. 16, which deals with *Dry Etching*.

WAFER CLEANING

Scrupulously clean wafers are critical for obtaining high yields in VLSI fabrication. Wafer cleaning is a complex subject as there are many possible kinds of contamination. In this section, the contamination types are listed, and then methods and equipment to remove them are described.

It should also be emphasized that if a source of contamination exists it may be more effective to eliminate the source of contamination, rather to remove the contaminant after it contacts the wafer. While cleaning procedures can remove an immediate problem, they represent additional processing steps which can possibly lead to even more contamination. In many instances eliminating contamination merely involves cleaning of process equipment.

Sources of Contamination and Their Detection on Wafer Surfaces

The two general categories of wafer contamination are particulates and films[1]. *Particulates* are any bits of material present on a wafer surface that have readily definable boundaries. As feature sizes shrink, the sizes of particulates that can cause defects also increase. Particulate sources include silicon dust, quartz dust, atmospheric dust, and particles originating from clean room personnel and processing equipment, lint (from street clothing that escapes from around protective clean room garments), photoresist "chunks" (e.g. resulting from tweezers gripping wafer edges), and bacteria (which can grow in DI water supplies).

Layers of foreign material on wafer surfaces are sources of *film contamination*. Portions of films may, however, break loose and become particles, as often happens with photoresist scums. Examples of films that contaminate wafers include *solvent residues* , such as acetone, isopropyl alcohol, methyl alcohol, xylene, *photoresist developer residues* from dissolved photoresist in the developer, or from inadequate post-development rinsing, *oil films* introduced through improperly filtered air or gas lines, and *metallic films* deposited during immersion of wafers in etchant or

resist stripper baths, both of which may contain metal ions and free metal in solution).

The chemical cleaning and photoresist stripping operations used to remove film contamination have also been identified as significant sources of particle contamination[2]. Thus, one stage of a cleaning process may in fact reduce the effectiveness of other cleaning procedures. To prevent particle contamination during chemical cleaning, the chemical process must be carefully monitored and particulate deposition effectively controlled. It is recommended, for example, that ultra-pure chemicals be utilized together with in-line point-of-use microfiltration for both chemical cleaning and resist stripping procedures[2,36].

In order to minimize wafer surface contamination and particulates, techniques to detect their presence must be available. For example, the concentration levels of particulates needs to be quantifiably measured after each process step. Only with such data in hand, can the effectiveness of the steps taken to reduce particulate counts be evaluated, and improved wafer cleaning procedures be implemented. Optical microscopy is used to detect particulates down to 1-2 μm in diameter, scratches, and solvent residues. Light-field, dark-field, Nomarski, and fluorescent illumination modes (see Chap. 17), are all useful for detecting such contamination and defects. Scanning electron microscopes are another tool used to analyze wafer surface contaminants.

Automatic laser scanners are also available for measuring surface defects and contamination (Fig. 1). Such instruments utilize a sharply focused laser beam and integrating light collector, to scan the entire wafer surface[3,4]. On a clean smooth surface, laser light is reflected at predictable angles, while any defects or contaminants on a surface cause light to be scattered. The light scattered by a defect is collected through a high efficiency light collection system. The scattered light is totally integrated by this optical system and then amplified by a photomultiplier tube. The output is a graphic display showing the number and type of defects. Such scanners can detect particles, pits, epi spikes, protrusions, cracks, scratches, and fingerprint residues of sizes as small as 1 μm in diameter. Total scanning time is on the order of a few seconds for a 100 mm

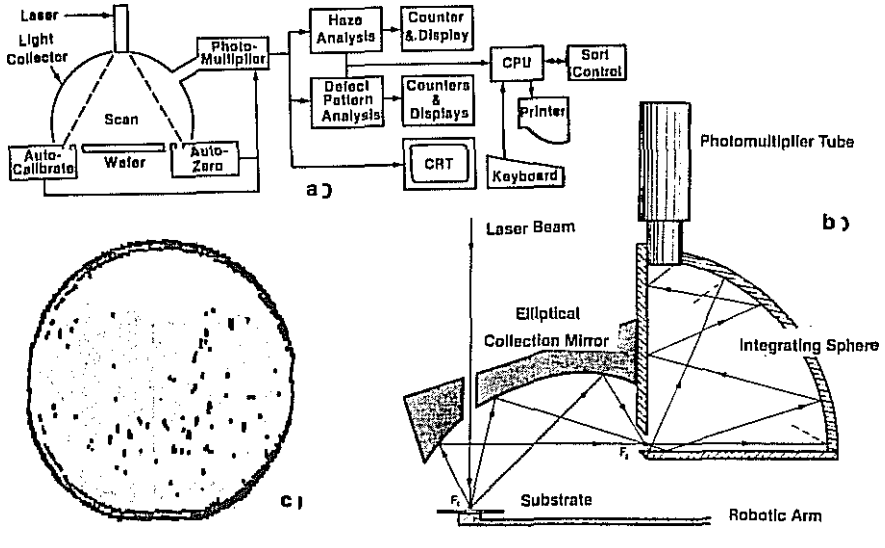

Fig. 1 (a) Functional block diagram of automatic defect detection system, utilizing a laser scanning detector. (b) Optical unit of the system (c) Typical surface patterns form an automatic laser scanning system. Courtesy of Tencor Instruments.

wafer. The major limitation of such systems is they are only effective on pattern-free substrates.

Surface analysis techniques such as Auger emission spectroscopy (AES) and secondary ion mass spectroscopy (SIMS) are capable of compositional analysis, typically elemental rather than molecular, of surface contaminant films, and in some cases of particulates (see Chap. 17). Such techniques are particularly useful for identifying the elemental composition of contamination which may have first been detected by other means.

Wafer Cleaning Procedures

As there are two classes of contamination, so there are separate cleaning procedures to remove each of them. That is, both chemical cleaning procedures and particulate cleaning techniques must be employed to produce a completely clean surface. As noted earlier, when one technique follows another, the latter steps must not recontaminate the surface and degrade the effectiveness of former cleaning procedures.

Chemical Removal of Film Contaminants

Chemical cleaning is used to remove chemically bonded films from wafer surfaces. Conventional chemical cleaning is performed with a series of acid and rinse baths. Many chemical cleaning processes are considered proprietary by device manufacturers, especially for some of the surfaces being cleaned (metal silicides, refractory metals, aluminum, and sputtered or deposited glasses). The chemical cleaning of silicon and silicon dioxide prior to high temperature operations, such as oxidation, diffusion, epitaxy, or anneal, however, is widely practiced according to the techniques presented here.

When bare silicon, or a silicon wafer with only thermally grown oxide, is chemically cleaned prior to a furnace step, the following procedure formulated by Kern and Puotinen at RCA[5], and hence often referred to as the *RCA method*, is widely used. The technique first removes organic film contamination and then applies an inorganic ion and heavy metal cleaning step. Note that the procedure outlined is adapted from Ref. 6, in which it is noted that a wide ranges of solutions in Steps 2 and 4 have also been successfully used.

1. *Preliminary Cleaning* - If photoresist is present on the wafers, it is removed by plasma oxidation stripping and /or immersion in an inorganic resist stripper (e.g. H_2SO_4-H_20_2). In many processes, even if the resist has previously been stripped, the first step of the cleaning is a second immersion into a sulfuric acid-oxidant mixture. Upon removal from this solution, the wafers are rinsed in 18-23°C deionized and filtered water, with a resistivity of 10-18 MΩ-cm. Such water is also used for all other rinse steps of this cleaning procedure.

2. *Removal of Residual Organic Contaminants and Certain Metals* - A fresh mixture of H_2O-NH_4OH-H_2O_2 (5:1:1 by volume) is prepared and heated to 75-80°C. The wafers and their holder are submerged in the solution for 10-15 minutes, with the temperature being maintained at 80°C. The wafers are then rinsed in DI water for one minute.

3. *Stripping of the Hydrous Oxide Film Formed During Step 2* (Note that this step is not necessary if a thermally grown SiO_2 film completely covers the wafer.) - Wafers are submerged for 15 seconds into a mixture of 1 volume HF (49% electronic grade) and 10 volumes H_2O directly from rinse tank of Step 2. Exposed silicon (but not SiO_2) should repel H_2O as the wafers are pulled out of this solution. Following immersion in HF, the wafers are transferred to a rinser, but are rinsed for only 20-30 seconds. The short rinse minimizes regrowth of the oxide. The holder and wafers are then transferred, without drying, into the solution of Step 4.

4. *Desorption of Remaining Atomic and Ionic Contaminants* - A fresh mixture of

Fig. 2 Single carrier rinser /dryer. Courtesy of Verteq Inc.

H_2O: HCl : H_2O_2 (6:1:1 by volume) is prepared and heated to 75-80°C. The still-wet wafers from Step 3 (or Step 2, if Step 3 is not necessary) are submerged into the solution for 10-15 minutes. The wafers are next rinsed in DI water to resistivity.

5. *Drying of Wafers* - Wafers are dried in a rinser-drier that uses DI water to rinse, and heated N_2 to dry. Remove wafers by dump transfer to a high-temperature boat.

6. *Storage* - Avoid storage of cleaned wafers, preferably by immediately continuing processing. If storage must occur, store in closed glass containers in a *nitrogen dry-box.*

Several other comments regarding this process are also pertinent. First, vapors of NH_3 and HCl form a particulate smoke of NH_4Cl when intermixed. It is therefore recommended that the solutions of Step 2 and 4 be separated by using two separate exhaust hoods, to avoid wafer contamination from colloidal NH_4Cl particles .

Second, reasonable care must be taken to prevent the cleaning solution of Step 2 from being depleted of H_2O_2, as NH_4OH in the absence of H_2O_2 will etch silicon. Such depletion may occur if the solution temperature is allowed to rise above 80°C, at which point rapid decomposition of the H_2O_2 ensues. In addition, if impurities are allowed to accumulate in the solution, they can also accelerate the decomposition of H_2O_2. Thus, use of fresh solutions is advised.

Third, the use of centrifugal spray cleaning instead of immersion in cleaning solutions is also favorably mentioned. In this method, the wafers are enclosed in a chamber purged with N_2. A sequence of fine sprays of cleaning solutions and high-purity water wets the wafers. The chief advantages of spray cleaning include: 1) smaller volumes of chemicals and DI water are consumed (about 2 /3 less); 2) wafer surfaces are continually exposed to fresh reagent solutions; 3) the environment of the process is carefully controlled; and 4) the process sequence is automated.

Finally, *dump rinsers* are used for DI water rinsing. In such rinsers, water is sprayed onto wafers and the cassette, filling the rinse tank at the same time. When the water reaches a predetermined level, doors at the bottom of the tank are opened and the water is quickly dumped. Several rinse /dump cycles are used, the exact number determined by the specific process, during a single rinse step. *Rinser-driers* are used to dry the wafers after the DI rinse step (Fig. 2). Modern

models typically hold one cassette of wafers. Following an initial spray rinse with DI water after the cassette is loaded, the wafers are spun dry while being sprayed with heated N_2. Static electricity may build up during the dry cycle and rinser-dryers can be equipped with static eliminators. In addition, loading and unloading of cassettes has been found to abrade the cassettes and generate particulates, and alternative drying techniques are therefore being explored.

Photoresist Removal

Photoresist must be removed following a wide variety of processing steps, including etching (wet and dry), ion implantation, lift-off processes, high temperature postbake (for improving resist adhesion or etch resistance), or merely simple removal of misaligned resist patterns for reimaging after development and inspection ("rework"). In addition, wafer surface patterns of several different materials may be present under the resist (e.g. SiO_2, aluminum, polysilicon, silicides, deposited SiO_2 or Si_3N_4 or polyimide). The main objective in resist stripping is to insure that all the photoresist is removed as quickly as possible without attacking any underlying surface materials[1]. In fact no single resist stripping chemical or technique is suitable for all applications. Resist stripping techniques are thus divided into three classes: 1) organic strippers; 2) oxidizing-type (inorganic) strippers; and 3) dry type stripping techniques.

Organic strippers perform resist removal by breaking down the structure of the resist layer. Commercially sold phenol-based strippers (such as *J-100*® by Indus-R-Chem, and *A20*® by Allied Chemical) were once quite popular, but their use is becoming more limited due to their relatively short pot life and the problem of phenol disposal[7]. In addition, some phenol-based strippers will attack metals. A class of low-phenol and phenol-free organic strippers (such as *Burmar 712*® [EKC Chemical], *Ecostrip*® [Allied Chemical], or *Remover 1112A*® [Shipley]) have been formulated to overcome these drawbacks. That is, they are safer to use and easier to dispose, although some may still attack aluminum to a limited degree.

Oxidizing-type strippers (wet inorganic) are solutions of H_2SO_4 and an oxidant, heated to ~125°C. They are used to remove resist from non-metallized wafers. The oxidant originally used was H_2O_2. It oxidizes the carbon in the resist to CO_2, which leaves the bath as a gas. H_2O_2, however, decomposes into water, making it difficult to maintain baths of consistent composition. As a result, *ammonium persulfate* has been suggested as an alternative to H_2O_2. Ammonium persulfate also liberates the carbon in the bath, but does not decompose into H_2O to dilute the H_2SO_4. This substantially increases bath life compared to H_2O_2. Oxidizing-type strippers are also commonly used to provide residue free removal of postbaked and other difficult-to-remove resists (e.g. those exposed to heavy ion implant doses or harsh dry etch environments).

Dry etching of resist is done using oxygen plasmas in plasma etching equipment. It offers several advantages over wet resist strippers including safer operating conditions, no metal ion contamination, reduced pollution problems, and no attack of most underlying substrate materials. Dry etching of organic films, including resist, is discussed in further detail in Chap. 16.

Wafers with defective photoresist imaging are frequently "reworked". In this process the photoresist is typically stripped with a commercially available stripper and then subjected to either: 1) a short dip in a 10:1 H_2O : HF solution and DI water rinse and dry; or 2) a 20 minute immersion in an 80°C solution of 7:3:3 (by volume) H_2O : H_2O_2 (30%) : NH_4OH (29%) and DI water rinse and dry[8]. These two post-strip steps are used to remove the monolayer of resist that usually remains after stripping, and which may lead to subsequent resist adhesion failure.

Photoresist may also remain attached to the *edge* of a wafer even after a conventional resist stripping process. It has been reported that failure to remove such resist clinging to the wafer edge, can cause significant defects. That is, such resist may later flake off and thus become a source of particulates. Reference 9 discusses the problem, and suggests a process of flowing a

solvent off the back of slowly rotating wafers, immediately afer spin-coating with resist, to thereby dissolve resist on the wafer edge (and remove the resist edge bead).

Cleaning Techniques for Removal of Particulates

The removal of insoluble particulate contamination is commonly carried out by ultrasonic scrubbing, or by techniques combining high pressure spraying and mechanical scrubbing. In *ultrasonic scrubbing*, wafers are immersed in a suitable liquid medium to which sonic energy (at 20,000-50,000 Hz) is applied[33]. Microscopic bubbles in the liquid medium are rapidly formed and collapsed under the pressure of the sonic agitation, producing shock waves which impinge on wafer surfaces. The bubble collapsing is known as *cavitation*. These shock waves displace or loosen particulate matter. To prevent shock waves from carrying particles from the liquid back to wafer surfaces and redepositing them, the particles must be removed from the liquid through overflow or filtration after they are initially detached. Another problem also observed is mechanical failure of the substrate film as a result of the ultrasonic energy imparted during the cleaning cycle. This frequently results in film loss in certain regions, and in the extreme, the entire film may be removed.

Cleaning systems using higher frequency sonic waves (~850kHz) are also commercially available (Fig. 3a). They can be operated with solutions used in the RCA chemical film removal process. With such systems chemical cleaning and contaminant desorption can be accomplished while simultaneously removing particulates.

Particulate removal by the combination of high pressure spraying and brush scrubbing is also commonly carried out *after* a variety of process steps (e.g. sawing, lapping, and polishing), and *before* others (e.g. metallization, CVD, and epitaxy [double-sided scrubbing]).

The scrubbing process operates by rotating a brush across the surface of wafers (Fig. 3b). It cleans by imparting motion to appropriate solvents, and the moving solvent dislodges particulates. In fact, the brush hydroplanes over, and does not actually contact the wafer surface. Two types of brushes are in common use: bristle and PVC sponge material. High pressure jet spraying is also almost always used with brush scrubbing. The high pressure, 13.8-20.7 MPa

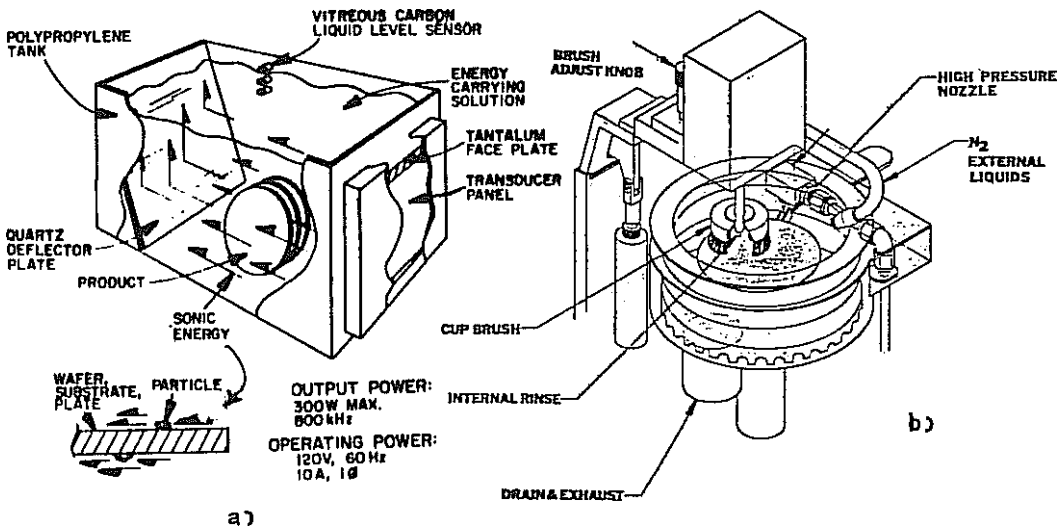

Fig. 3 (a) Megasonic wafer cleaning system. Courtesy of Verteq Inc. (b) Diagram of a cup-type brush cleaning station. Courtesy of Solitec Inc.

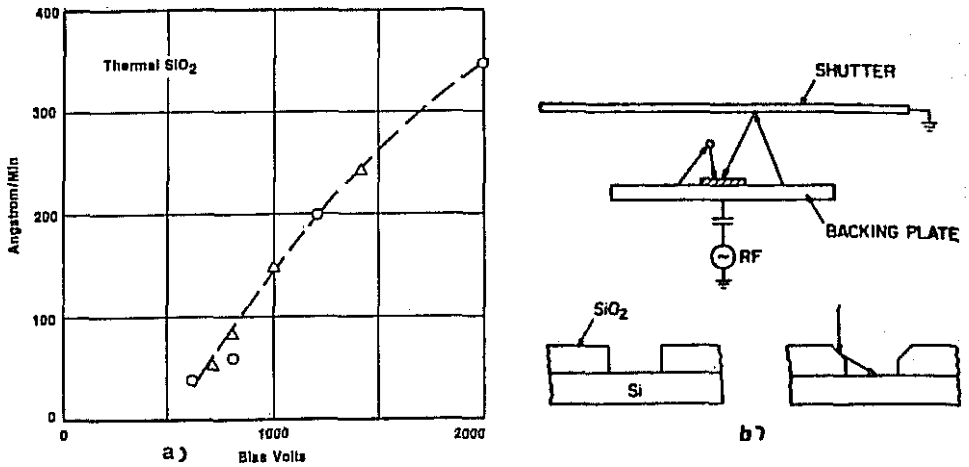

Fig. 4 (a) Example of sputter-etch rate of thermal SiO_2. Courtesy of Varian Associates. Contamination of contacts during sputter etching by (b) backscattering events, and (c) faceting. Material sputtered from the facet deposits in the contact at a rate that can exceed removal of material from the bottom of the opening[10]. Reprinted by permission of the American Physical Soc.

(2000-3000 lb /in^2) DI water jet sweeps across the wafer surface and removes the microscopic debris dislodged by the brush, as well as any residual particles generated by the brush.

In-Situ Sputter Etch Removal of Native Oxide Films

A thin oxide (5-50 Å) grows on silicon (SiO_2) or aluminum (Al_2O_3) when these materials are exposed to air. This thin oxide (known as *native oxide*) can adversely effect subsequent processing steps, for example by causing high contact resistance, or impeding interfacial reactions of films deposited on the substrate materials. Thus, it is important to remove this oxide layer and keep it from reforming before depositing the overlying film.

Concerns have arisen about whether chemical cleaning techniques will be adequate for removing native oxide films, especially in contact holes or via regions smaller than 2 μm. As a result removal of such films is also being conducted in the same vacuum environment in which the overlying film will be deposited (*in situ*). Sputter etching is used to remove up to several hundred angstroms of the wafer surface including, it is surmised, the unwanted native oxide at the bottom of the contacts or vias. Some questions have also been raised about the effectiveness of this technique for small (e.g. < 2 μm) contacts[10]. It is argued that such sputter etching (Fig. 4) will cause more contamination of the contacts through redeposition by backscattering of material sputtered from wafers and chamber surfaces, and by sputtering of contact sidewall material into the contact bottom. *In situ* removal of the native oxide by plasma chemical reactions, instead of physical sputtering mechanisms, has been proposed to circumvent this problem. Several sputter equipment suppliers offer such alternative *in situ* cleaning capabilities.

TERMINOLOGY OF ETCHING

Etching in microelectronic fabrication is a process by which material is removed from the silicon substrate or from thin films on the substrate surface. When a *mask layer* is used to protect specific regions of the wafer surface, the goal of etching is to precisely remove the

material which is not covered by the mask (Fig. 5). In this section we will discuss the terms used to describe the basic aspects of etch processes.

Bias, Tolerance, Etch Rate, and Anisotropy

In general an ideal etch process is not completely attainable. That is, the etching processes are not capable of precisely transferring the pattern established by the protective mask into the underlying material. The degree to which the process fails to satisfy the ideal is specified by two parameters: *bias* and *tolerance*. As shown in Fig. 6d, *bias* is the difference in lateral dimension between the etched image and the mask image. *Tolerance* is a measure of the statistical distribution of bias values that characterizes the uniformity of etching. The tolerance parameter can be specified for a single wafer (bias distribution across a wafer), for an entire lot (bias distribution throughout the lot) or from run-to-run (bias distribution across a group of runs).

The rate at which material is removed from the film by etching is known as the *etch rate*. The units of etch rate are typically expressed in Å /sec, μm /min, etc. Generally, high etch rates are desirable as they allow higher production throughputs, but in some cases high etch rates make control of lateral etching a problem. That is, since material removal can occur in both the horizontal and vertical directions, the *horizontal etch rate* as well as the *vertical etch rate* may need to be established in order to characterize an etch process. Normally the uniformity of these etch rates is also of interest, and is expressed for three conditions (across a wafer, from wafer-to-wafer, and from run-to-run), as *etch rate % uniformity*, according to:

$$\text{Etch Rate Percent Uniformity} = \frac{(\text{Etch Rate}_{high} - \text{Etch Rate}_{low})}{(\text{Etch Rate}_{high} + \text{Etch Rate}_{low})} \times 100\% \qquad (1)$$

Highly uniform etch rates are almost always desirable in an etch process.

The lateral etch ratio, L_R, is defined as the ratio of the etch rate in a horizontal direction to

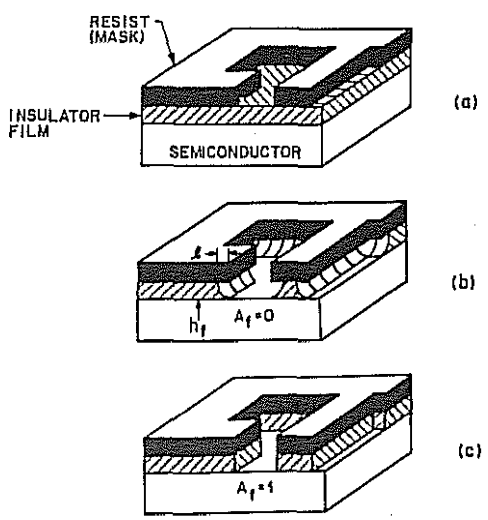

Fig. 5 Comparison of (b) isotropic, and (c) completely anisotropic etching. From E.C. Douglas, *Solid State Tehnol.*, 24, 65, (1981). Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet.

that in the vertical direction. Thus:

$$L_R = \frac{\text{Horizontal Etch Rate of Material}}{\text{Vertical Etch Rate of Material}} \quad (2)$$

In the case of an ideal etch process the mask pattern would be transferred to the underlying layer with zero bias. This would then create a vertical edge profile in the etched layer coincident with original edge of the mask. Therefore the lateral etch rate would also have to have been zero. For non-zero L_R, the film material is etched to some degree under the mask and this effect is called *undercut* (Fig. 5d).

When the etching can proceed in all directions at the same rate, it is said to be *isotropic* (Fig. 5b). By definition, however, any etching that is not isotropic is *anisotropic*. If etching proceeds exclusively in one direction (e.g. only vertically), the etching process is said to be *completely anisotropic*. Since many etch processes fall between the extremes of being isotropic and completely anisotropic, it is useful to define a degree of anisotropy, A, as:

$$A = 1 - L_R \quad (3)$$

Thus, when $L_R = 0$, $A = 1$, and this condition corresponds to completely anisotropic etching. When $L_R = 1$, the vertical and horizontal etch rates are equal, and the degree of anisotropy is $A = 0$. This corresponds to an isotropic etching condition. Most wet etching processes and some dry-etching processes exhibit uniform etch rates in all directions, and hence are isotropic.

An example of an etch profile in the film being removed versus time is shown for an isotropic etch, $L_R = 1$ (Fig. 6a) and for a process in which $L_R = 0.1$ (Fig. 6b). If the films are etched just to completion, the profile for $L_R = 1$ has the shape of a quarter circle, whereas the profile of $L_R = 0.1$ is vertical except near the bottom (where it is rounded). If this etch is allowed to continue, however, even the profile with $L_R = 1$ becomes more vertical, though

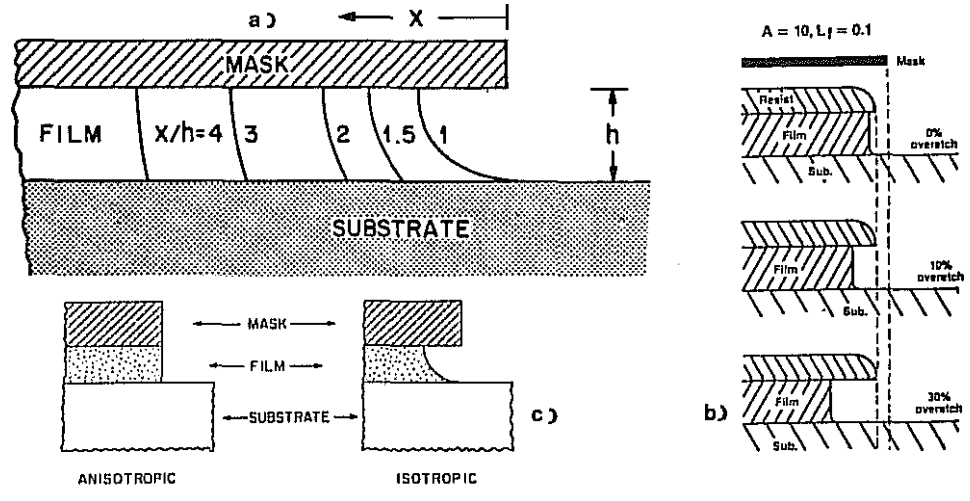

Fig. 6 (a) Isotropic etching of a film vs time ($L_R = 1$). Overetching results in profiles are more vertical. (b) Etching of film versus time when $L_R = 0.1$. (c) Etch bias is a measure of the amount by which the etched film undercuts the mask at the mask film interface. Fig. (c) Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted by permission.

lateral etching proceeds more rapidly than the process in which $L_R = 0.1$, and thus leads to more severe undercutting. As a result, we see that L_R is one of the variables which impacts feature size, as well as edge profile. We shall also see that other parameters play a role in controlling such characteristics of the feature attributes as size and edge profile.

In fabrication technologies that are performed using isotropic etching processes, the problem of etch bias is handled by specifying an appropriate amount of compensation in the mask dimensions. For example, if the bias of an etch process is 1 μm, a 6 μm feature on the *mask* can be used to produce a desired 5 μm feature on the *wafer*. Unfortunately, for VLSI technologies in which the pattern dimensions approach the thicknesses of the films being patterned, the margin for compensation diminishes, and a higher degree of anisotropy is required. For practical purposes this situation arises when pattern features become smaller than ~3 μm. Under these circumstances, isotropic etching processes become inadequate, and processes that provide higher degrees of anisotropy need to be employed.

Selectivity, Over-Etch, and Feature Size Control

In earlier sections, only the etching characteristics of the film were considered when examining the relationship between bias and edge profile, and degree of etch anisotropy. We assumed that the mask was not attacked by the etchant, and did not consider that the layers under the etched film can also be attacked by the etchant. In fact, both mask material and underlying layer materials are generally etchable, and these effects may play a significant role in specifying etch processes. Note that the underlying material subject to etchant attack may be either the silicon wafer itself, or a film grown or deposited during a previous fabrication step. The ratio of etch rates of different materials is known as the *selectivity of an etched process*[12]. Thus both: 1) the selectivity with respect to the mask material; and 2) the selectivity with respect to the substrate materials are important characteristics of an etch process.

The *selectivity with respect to the mask material*, S_{fm}, plays a role in determining the etched feature sizes. The *selectivity with respect to substrate*, S_{fs}, can impact performance and yield. Film thickness and etch rate non-uniformities increase the required values of S_{fm} and S_{fs} because the etch processes need to be continued beyond the point at which the mean film thickness is completely etched (cleared). Such additional etching is referred to as *overetch*. For example, due to overetch requirements, when contact holes are to be etched in SiO_2 it is desirable that the etch rate decrease when the silicon substrate is reached. In this case, a process with high selectivity with respect to substrate is necessary.

For many wet-etch processes, both S_{fm} and S_{fs} are very high, and thus neither the mask or substrate materials are affected very much during such well-controlled wet-etch procedures. However for dry-etch processes, these desirable circumstances are rarely encountered. Thus, it is necessary to calculate the selectivities that an etching application will require, so that dry-etch processes which are able to meet such specifications can be selected or developed.

Determining the Required Selectivity With Respect to Mask Materials, S_{fm}

The required selectivity with respect to the mask, S_{fm} is dependent on several factors including: a) film thickness uniformity; b) film etch rate uniformity; c) mask etch rate uniformity; d) the edge profile of the mask; e) the anisotropic etch rate of the mask; and f) the maximum acceptable loss of line width of the patterns being etched[11]. These factors can be quantified with the assistance of the information given in Fig. 7.

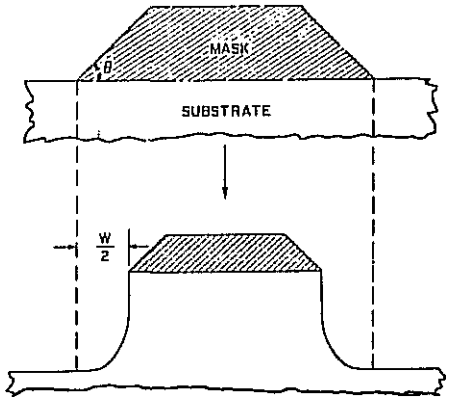

Fig. 7 The evolution of an etched feature when the mask has a finite etch rate. The difference between the intended pattern width and the actual linewidth is W. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted by permission.

For example, assume we wish to etch a film that has some degree of thickness non-uniformity. This film has a mean thickness, h_f, a maximum thickness, $h_f(1 + \delta)$, and a minimum thickness, $h_f(1 - \delta)$, where δ is a dimensionless parameter with a value $0 \leq \delta < 1$. Assume also that the film etch rate is somewhat nonuniform. That is, a mean etch rate, v_f, of the film exists over the wafer area, and that v_f varies between $v_f(1 + \phi_f)$ and $v_f(1 - \phi_f)$, where ϕ_f is again a dimensionless parameter of value $0 \leq \phi_f < 1$. In order to insure that the maximum loss of linewidth is less than or equal to the allowable linewidth loss, this effect must be determined for the worst-case etching condition on the wafer. Maximum linewidth loss occurs where the film is thickest, $[h_f(1 + \delta)]$, and at wafer locations where the film etch rate is slowest, $v_f(1 - \phi_f)$. Thus, the time required to etch the film at such locations is the longest, and is given by:

$$t_c = \frac{h_f(1 + \delta)}{v_f(1 - \phi_f)} \tag{4}$$

If it is independently determined that a fractional overetch time, Δ, is also required, then the total etch time, t_t, is increased to:

$$t_t = \frac{h_f(1 + \delta)(1 + \Delta)}{v_f(1 - \phi_f)} \tag{5}$$

During the etch time, the mask will be eroded as shown in Fig. 7. If the mask material is removed with maximum vertical and horizontal etch rates, v_v and v_l, respectively, then the edge of the mask will retreat from its original locations by a distance, W /2, given by:

$$\frac{W}{2} = [v_v \cot\theta + v_l] t_t \tag{6}$$

where θ is defined in Fig. 7, and the total loss of linewidth is 2(W /2). The loss of linewidth dimension of the mask, W due to erosion during t_t, is then found by substituting Eq. 5 into Eq. 6 to give:

$$W = 2\frac{v_v}{v_f}h_f\frac{(1+\delta)(1+\Delta)}{(1-\phi_f)}\left[\cot\theta + \frac{v_l}{v_v}\right] \qquad (7)$$

The mask etch rates are generally also nonuniform, and the nonuniformity is expressed as $v_v = v_m(1 \pm \phi_m)$, where v_m is the mean mask etch rate and ϕ_m is a dimensionless parameter. For the worst case again, we select the condition where the mask etch is fastest. Thus, $v_m(1+\phi_m)$ is substituted into Eq. 7 for v_v. In addition, selectivity with respect to the mask is defined as $S_{fm} = v_f/v_m$. From Eq. 3 the mask lateral etch rate ratio is $v_v/v_L = L_R = 1 - A_m$. Using these definitions and rearranging Eq. 7 we get the required S_{fm} as:

$$S_{fm} = \frac{h_f}{W}U_{fm}[\cot\theta + (1 - A_m)] \qquad (8)$$

where;

$$U_{fm} = \frac{[(1+\delta)(1+\Delta)(1+\phi_m)]}{(1-\phi_f)} \qquad (9)$$

and U_{fm} is the uniformity factor that accounts for the simultaneous occurrence of worst-case conditions that leads to the greatest mask erosion, and thus maximum linewidth loss. Figure 8 shows a set of curves of required S_{fm} which apply to the specific case of $\phi_m = \phi_f = 0.1$, $\delta = 0.05$, and $\Delta = 0.2$. For these conditions $U_{fm} = 1.54$, and the curves are plotted for various h_f/W ratios and various degrees of mask edge angles, θ, and etch anisotropy, A.

Example: Assume that a 1 μm film is to be patterned with a completely anisotropic etch process and thus the only loss of feature linewidth is due to mask erosion. In addition, let the mask and film etch rate uniformities both be 10%, and the film thickness uniformity be 5%. In addition, a 20% overetch is required. Find the required selectivity to the mask for a maximum 0.2 μm linewidth loss if the resist profile angle is, a) 60%, and b) 90% for, 1) isotropic mask etching, and 2) completely anisotropic mask etching.

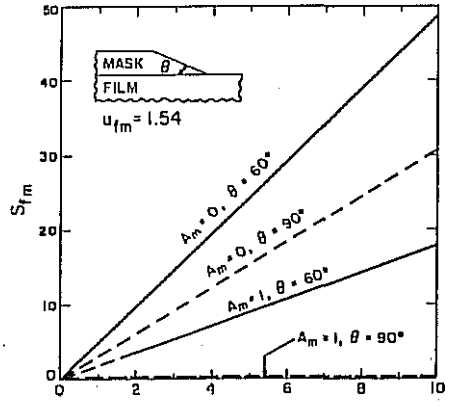

Fig. 8. Selectivity, S_{fm}, needed with respect to the mask, plotted as a function of the ratio of film thickness to loss of linewidth for various mask profiles, and the extremes of isotropic & anisotropic mask etching. Copyright 1983 Bell Telephone Laboratories, Inc, reprinted by permission.

Solution: Figure 8 can be used to solve this problem since the curves were generated for the given worst case nonuniformity values from Eq. 8. Note that for other etch rate and thickness non-uniformities, different curves need to be derived. For this film $h_f = 1.0$ μm, and $W = 0.2$ μm, so $h_f/W = 5$. From the curves of Fig. 7 we see that the following S_{fm} are required:

a) $S_{fm}(\theta = 60°, A = 0) = 23$
b) $S_{fm}(\theta = 60°, A = 1) = 9$
c) $S_{fm}(\theta = 90°, A = 0) = 15$
d) $S_{fm}(\theta = 90°, A = 1) = 0$

It can be seen from this example that anisotropic etch processes, combined with vertical walled etch mask profiles, result in the most precise pattern transfers. However, there is also another phenomenon associated with sputtering and dry-etching, referred to as *faceting* which can also contribute to mask erosion. Faceting is discussed in more detail Chap. 10.

Determining Required Selectivity With Respect to Substrate, S_{fs}

The necessary selectivity with respect to substrate, S_{fs}, is also calculated by considering the worst-case condition[13]. That is we assume the thinnest part of the film to be etched lies over the region of the substrate that experiences the highest etch rate. We use this assumption to calculate a uniformity factor, U_{fs}. We then multiply U_{fs} by the ratio h_f/h_s (where h_f is the mean film thickness, and h_s is the maximum allowable penetration depth of the substrate layer) to arrive at the required S_{fs}, or:

$$S_{fs} = \frac{h_f}{h_s} U_{fs} \qquad (10)$$

and

$$U_{fs} = \left[\frac{\phi_f(2 + \Delta + \Delta\delta) + \delta(2 + \Delta) + \Delta}{(1 - \phi_f^2)} \right] \qquad (11)$$

where ϕ_f, Δ, and δ are defined as in the last section that derived S_{fm}. We see from Eq. 10 that if the film is perfectly uniform ($\delta = \phi_f = 0$) and if no overetching is required ($\Delta = 0$), selectivity with respect to the substrate would not be an issue of concern since U_{fs} would equal zero. However, since these conditions are not representative of actual conditions, Eq. 10 is useful in *determining realistic* S_{fs} values.

There is another factor, even more important than film and etch rate non-uniformities, which dictates the degree of overetching when anisotropic etch processes are employed. That is, as shown in Fig. 9a, when material is cleared from a planar region on a wafer, residual material at steps has still not been removed. Thus, additional etching beyond the point at which the planar regions have cleared must be used to remove such residual material (sometimes referred to as *stringers* or *picket fences*). As shown in Fig. 9b, failure to remove this material can lead to unwanted electrical shorting paths between adjacent lines. From Fig. 9a and b, it can be seen that for completely anisotropic etch processes (A = 1), the fractional overetch, Δ, required to clear such residual material, is h_1/h_2.

Example: Given a 2500 Å polysilicon layer that passes over both 5000 Å field-oxide regions and 250 Å gate oxide layers. Assume that a completely anisotropic

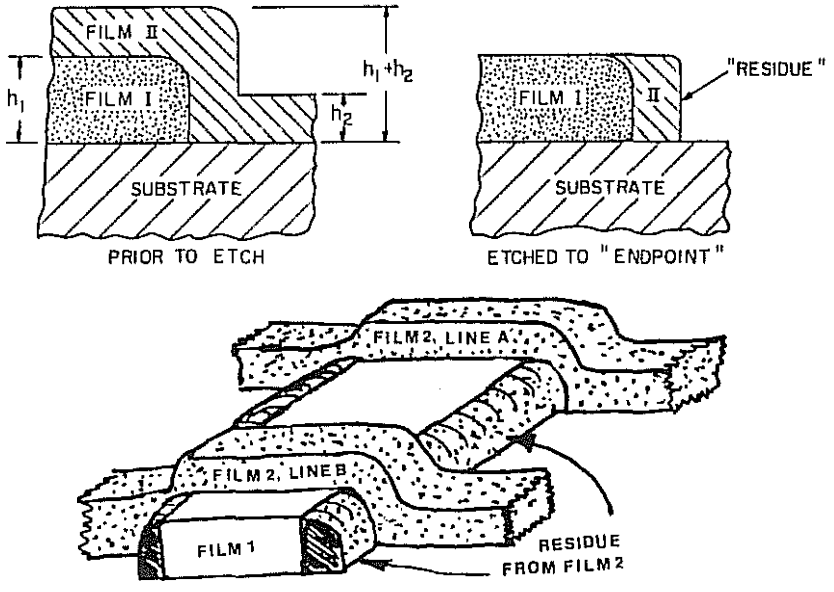

Fig. 9 If etching is anisotropic, overetching is needed to remove residual materials at steps. The degree of anisotropy, A = 1 in the example shown. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted by permission.

etch process will be used to etch the polysilicon, and that the polysilicon film thickness uniformity is 5%, and the uniformity of etching is 10%. Find the required S_{fs} for this process, if the etching is to be stopped immediately after the polysilicon is completely etched.

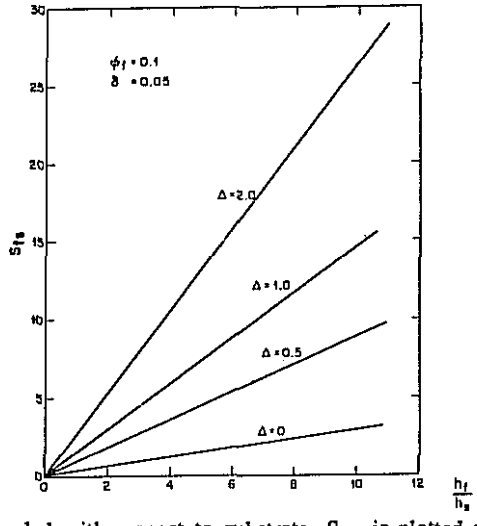

Fig. 10 The selectivity needed with respect to substrate, S_{fs}, is plotted as a function of the ratio of film thickness to the amount of substrate removed for various amounts of overetching. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted by permission.

Solution: Since the polysilicon must pass over 5000 Å steps (e.g.where field and gate oxide meet), the thickness of the poly at the step will be (from Fig. 8):

$$h_1 + h_2 = 5000\ \text{Å} + 2500\ \text{Å} = 7500\ \text{Å}.$$

This is the thickness of polysilicon that must be removed by an anisotropic etch procedure. Thus, $\Delta = h_1/h_2 = 2$. The maximum allowable penetration of the fractional overetch required to completely remove the residual material at the steps underlying gate oxide layer is $h_s = 250$ Å. Any more penetration will remove all of this oxide and expose the silicon substrate material to the etchant. Thus, $h_f/h_s = 2500/250 = 10$. From Fig. 10, which can be applied to this problem, we find that:

$$S_{fs} = 25.$$

Note the curves of Fig. 8 and Fig. 10 were derived for specific mask, film, and etch rate nonuniformities. Each etching process, however has its own set of characteristics and appropriate curves for a specific process need to be derived using Eq. 8 and Eq. 10 with those values.

Combined Impact of the Requirements of Anisotropy and Selectivity

A high degree of anisotropy is a desirable feature of an etch process for fine feature patterning since in such applications very little etch bias can be permitted. A highly selective etch rate with respect to the mask is needed to maintain feature size control. An adequate degree of selectivity with respect to underlying materials is also necessary in order to prevent removal of previously processed portions of the circuit. However, when anisotropic etching is performed in the presence of stepped topography, we have shown that the remaining residual material at the steps requires additional overetching beyond even that required by etch rate and "normal" film thickness nonuniformities. Thus, the mandate that calls for anisotropic etch processes ends up also driving the selectivity requirements even higher.

Loading Effects

When the etch rate is dependent upon the amount of etchable surface exposed to the etchant, the phenomenon is called a *loading effect*. The effect arises when there are a limited number of etchant species available to etch a material. When these are depleted, etching cannot continue until new etching species arrive at the surface. Loading effects are most commonly encountered in dry-etch processes where they can occur in a variety of different conditions. These include: a)

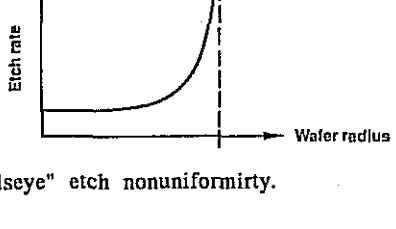

Fig. 11 Example of "bullseye" etch nonuniformirty.

etch rate is dependent upon the number of wafers present in the chamber. In such cases, as the number of wafers in the system is increased, the rate of consumption of etchant species also increases. This may result in a loading effect that will lead to a slower overall etch rate; b) the etch rate depends on the amount of area on the wafers, or on a single-wafer in single-wafer etching systems, that has etchable material exposed. Note that this exposed etchable area can even change during an etch process. That is, upon the clearing of an etching film from the planar regions of a surface, much less residual material remains. Thus, more etchant species may be available to attack any residues, but also the exposed sidewalls of the etchable film. As a result, lateral etch rate changes during overetch time may be a side effect of local loading effects.

Gas flow effects may also combine with loading effects to cause etch rate nonuniformities. That is, the location of a wafer in a chamber, as well as the number present in the chamber, may impact the etch rate. The *bullseye effect* sometimes observed in dry etching, in which the film at edges of a wafer is etched more quickly than at the center (Fig. 11), is due to depletion of etchant species at the wafer center. More etchant species can arrive at the wafer near its edge than from just above the wafer surface. Techniques to minimize loading effects are described in Chap. 16.

WET ETCHING TECHNOLOGY

Wet etching processes are generally isotropic. As such we have pointed out that they are inadequate for defining features less than about 3 μm wide. Nevertheless for those process that involve patterning of linewidths greater than 3 μm, wet etching continues to be a viable technology. Since it turns out that a significant fraction of semiconductor products are still being fabricated with such large geometries, wet etching should not be ignored. In this section we present some of the more important aspects of wet etching technology for current processing needs. In addition more detailed information can be found in references listed at the end of the chapter[1,14,17,18,10].

The reason wet etching has found widespread acceptance in microelectronic fabrication is that it is a low cost, reliable, high throughput process with excellent selectivity for most wet etch processes, with respect to both mask and substrate materials. Some recent refinements to wet-etching equipment have in fact increased these advantages, including: a) the automation of wet stations; b) the placing of wet etch process steps under microprocessor control, to improve reproducibility of etching conditions from run-to-run, and to give the process engineers better control of the equipment functions by preventing unauthorized process changes; c) point-of-use filtration of etchants to prolong their use by removing etch process generated defects; and d) the development of spray etching. Such advances make it likely that wet etching will continue to find extensive use in semiconductor fabrication for the foreseeable future[15,16].

On the other hand, besides the 3 μm limitation, wet etching is subject to the following disadvantages: a) higher cost of etchants and DI water compared to dry etch gas expenses; b) increased personnel safety hazards from chemical handling; c) exhaust fumes and the potential of explosions; d) resist adhesion problems; and e) bubble formation and incomplete wetting of wafer surfaces by the chemical etchants leading to incomplete etching and etching non-uniformities.

In general a wet etch process can be broken down into three steps: 1) diffusion of the reactant to the reacting surface; 2) reaction; and 3) diffusion of the reaction products from the surface[20]. The second step can obviously be further differentiated into adsorption prior to, and desorption subsequent to, the actual reaction step. The slowest of the steps will be *rate-controlling*. That is, the rate of that step will be the rate of the overall reaction.

Chemical etching can occur by several processes. The simplest involves dissolution of the

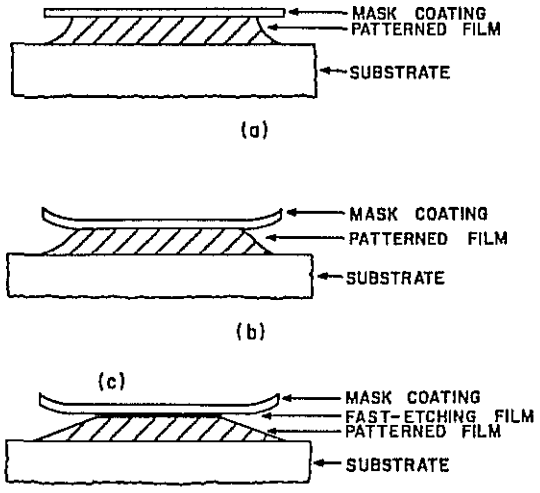

Fig. 12 Different etch profiles produced from various degrees of undercutting during wet etch. (a) Good mask-to-film adhesion. (b) Undercutting has occurred at mask-film interface. (c) Use of fast-etching film to achieve controlled undercutting[14]. Reprinted with permission of Academic Press.

material in a liquid solvent without any change in the chemical nature of the dissolved species. Most etching processes, however, involve one or more chemical reactions (Step 2 above). Various types of reactions may take place, although one commonly encountered in semiconductor fabrication is oxidation-reduction (redox). That is, a layer of oxide is formed, then the oxide is dissolved and the next layer of oxide is formed, etc (e.g. in wet etching of Si and Al).

In semiconductor applications, wet etching is used to produce patterns on the silicon substrate or in thin films. A mask is typically used to protect desired surface regions from the etchant and this mask is stripped after the etching has been performed. Thus, when choosing a wet etch process, in addition to selecting an etchant, a suitable masking material must be picked to have good adhesion to the underlying films, good coating integrity and the ability to withstand attack by the etchant. Photoresist is the most commonly encountered masking layer, but sometimes it falls short in this role. Problems encountered with photoresist as a mask layer in wet etching applications include loss of adhesion at the edge of the mask-film interface due to etchant attack (Fig. 12), and large area failure of the resist. Edge attack is combatted by use of adhesion promoters such as hexamethyldisilazane (HMDS). Large area failures of resist are usually due to differential stress buildups in the substrate and mask layers. Such problems are minimized by using mask materials with enough elasticity to conform to stresses between mask and substrate (that build up from differential coefficients of expansion).

Etching processes which produce bubbles can also lead to poor pattern definition due to the clinging of such bubbles to the substrate, particularly along the pattern edges. Bubbles deny the etchant local access to the film being etched, and at those locations etching temporarily slows down or ceases, until the bubble is dislodged. Therefore, use of wetting agents in the etchant together with agitation during etching are measures taken to assist in dislodging such bubbles.

Developer residue or *scum* is also a common cause of etch blocking in which non-etching or poor wetting of the etchant is observed. The two most common causes are: 1) developer baths that have had their active ingredients depleted; and 2) underexposed resist. When the developer is no longer at full strength, it may not completely remove the exposed positive resist, and a thin resist layer is left behind. Such residual layers are very difficult to detect prior to etching.

Therefore, to avoid such problems it is necessary to use fresh developer after a specific number of wafers have been processed in the bath, in batch immersion development processes. In addition, a descum step, using an oxygen plasma, is used to remove such residues (see Chap. 12).

We will now discuss wet-etching aspects of the most commonly encountered materials which are etched in the microelectronic fabrication environment: silicon; silicon dioxide; silicon nitride; and aluminum.

Wet Etching Silicon

Both single crystal and polycrystalline silicon are typically wet etched in mixtures of nitric acid (HNO_3) and hydrofluoric acid (HF). The reaction is initiated by the HNO_3 which forms a layer of silicon dioxide on the silicon, and the HF dissolves the oxide away. The overall reaction is:

$$Si + HNO_3 + 6\,HF \rightarrow H_2SiF_6 + HNO_2 + H_2 + H_2O \qquad (12)$$

Water can be used to dilute the etchant, but acetic acid (CH_3COOH) is preferred as a buffering agent, since it causes less dissociation of HNO_3, and thus yields a higher concentration of the undissociated species.

The mixture compositions can be varied to yield different etch rates. Figure 13 shows the isoetch curves of such mixtures for various constituents by weight[21]. We see that at high HF and low HNO_3 concentrations (the region near the upper corner of the triangle), the etch rate is controlled by the HNO_3 concentration, because in such mixtures there is an excess of HF to dissolve the SiO_2 created during the reaction. On the other hand at low HF and high HNO_3 concentrations, the etch rate is limited by the ability of the HF to remove the SiO_2 as it is created. In such etchants the etching is isotropic, and they are often used as polishing agents.

In some applications, it is useful to etch silicon more rapidly along some crystal planes than others[22]. This allows the etch to significantly slow down or to etch specific shapes or structures in the silicon. In the diamond lattice we observed that the (111)-plane is more densely packed than the (100)-plane, and thus the etch rates of (111)-oriented surfaces are expected to be lower than those with (100)-orientations. An etchant that exhibits such orientation-dependent

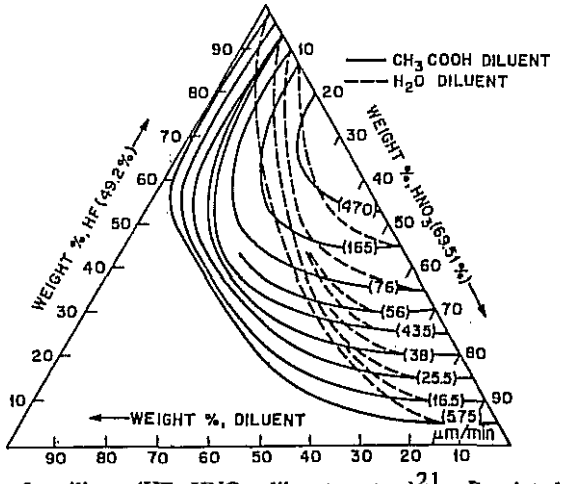

Fig. 13 Isoetch curves for silicon (HF: HNO_3 diluent system)[21]. Reprinted with the permission of the publisher, the Electrochemical Society.

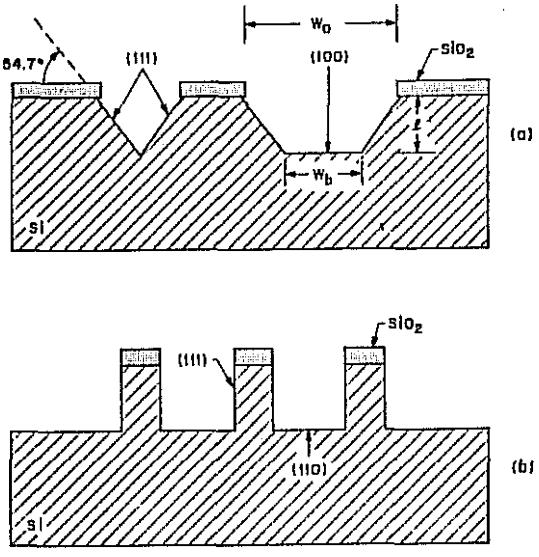

Fig. 14 Orientation-dependent Si etching (a) etch pattern profiles on <100>-Si, (b) etch pattern profiles on <110>-Si[22]. (© 1978 IEEE).

etching properties in silicon consists of a mixture of KOH and isopropyl alcohol (e.g. 23.4 wt % KOH, 13.3 wt % isopropyl alcohol, and 63 wt % H_2O). The etch rate of this etchant is about 100 times faster along (100)-planes than along (111)-planes (e.g. at 80°C, 0.6 μm /min vs. 0.006 μm /min).

If features in a (100)-plane of silicon are patterned with SiO_2, this orientation-etchant will create precise V-shaped grooves in the silicon, and the edges of the grooves will be (111)-planes at an angle of 54.7° from the (100)-surface (Fig. 14a). If (110)-surfaces are used, straight-walled grooves with sides having (111)-planes are formed (Fig. 14b).

Various etchant mixtures have also been devised to allow the delineation of crystalline defects in silicon. Most defect analysis using such wet chemical etchants utilizes one of three formulations which are listed in Table 1. The Sirtl etch[23] is fast and effective for (111)-surfaces, but tends to cause clouding and thereby produces confusing results on (100)-surfaces[30]. The Secco[24] and Wright[25,29] etches provide better results for these applications.

Wet Etching Silicon Dioxide

Wet etching of SiO_2 films in microelectronic applications is usually accomplished with various hydrofluoric acid (HF) solutions[17,20]. This is because SiO_2 is readily attacked by room temperature HF, while Si is not. Etching takes place according to the overall equation:

$$SiO_2 + 6HF \rightarrow H_2 + SiF_6 + 2\,H_2O \qquad (13)$$

The concentration of HF supplied by chemical manufacturers is 49% in water. Such concentrated HF, however, etches SiO_2 too quickly for good process control (e.g. thermally grown SiO_2 is etched at approximately 300 Å /s at 25°C). Thus diluted HF is generally used instead. A common etchant formulation contains buffering agents such as ammonium fluoride (NH_4F), which help prevent depletion of the fluoride ions, and thus maintain stable etching characteristics.

Table 1. ETCHES FOR DEFECT ANALYSIS ON SILICON WAFERS

Etch	Formulation	Comments
1. Sirtl [4]	50g CrO_3 to 100 ml H_2O.	Fast, good defect analysis on (111) material.
	Mix 1:1 with 48% HF prior to use.	Develops stains and cloudy surfaces on (100) making interpretation difficult.
2. Secco [5]	44g $K_2Cr_2O_7$ to 1000 ml H_2O.	Good delineation of defects on (100) surfaces.
	Mix 1:2 with 48% HF.	Slower etch rates.
		Requires ultrasonic agitation to avoid bubble formation.
3: Wright [6]	2g Cu $(NO_3) \times 3H_2O$ in 60 ml H_2O.	Good for both (100) and (111) surfaces.
	Add:	
	60 ml 48% HF	Moderate Etch rate.
	30 ml 69% HNO_3	Minimum of etch anomalies.
	30 ml 5 $MCrO_3$ (1g CrO_3/2 ml H_2O)	Useful for wafer cross-sections.
	60 ml acetic acid	For mulation is complex.

Unbuffered HF also causes both excessive undercutting at the resist oxide interface and lifting of the resist. A typical buffered HF mixture (BHF) contains 6:1 (by volume) NH_4F:HF (40%:49%) which etches thermally grown SiO_2 at ~20 Å /sec (or ~1000 Å /min) at 25°C.

The etch rate of SiO_2 for a given etchant and temperature, also depends on several other factors. For example, SiO_2 thermally grown in steam etches slightly faster than SiO_2 grown in dry O_2. The presence of impurities in the oxide can also strongly affect the etch rate. A high concentration of boron results in a reduced etch rate, while a high concentration of phosphorus rapidly increases it. Ion implantation can produce damage that will increase the SiO_2 etch rate.

CVD SiO_2 (Chap. 6), generally etches much more rapidly than thermally grown SiO_2, but this rate also depends on many other factors[26], including deposition conditions, impurity concentration, and densifying heat treatments after deposition. As a general rule, SiO_2 films deposited at low temperatures exhibit higher etch rates than films annealed or deposited at higher

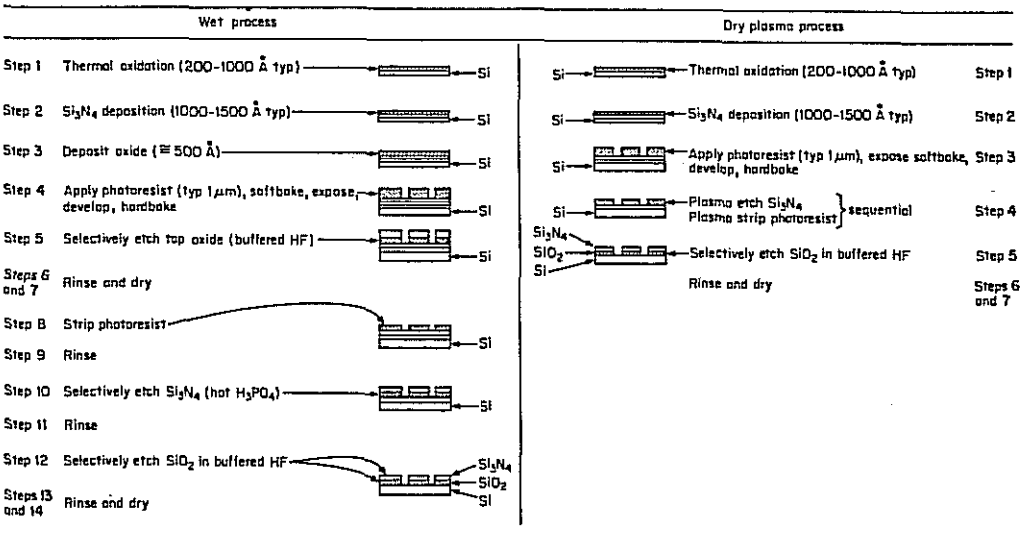

Fig. 15 Wet vs. dry-etch process for Si_3N_4. Courtesy of L.F.E. Corp., Plasma Systems Group.

temperatures. CVD SiO_2 is more commonly etched in diluted HF etches, since slower and more controllable etch rates can be achieved (e.g. 10:1-100:1 H_2O:HF).

Wet Etching Silicon Nitride

Silicon nitride (Si_3N_4) can be etched by reflux boiling 85% phosphoric acid at 180°C[17]. However photoresist is lifted during such etching and does not make a good etch mask for this application. Most wet silicon nitride etching thus utilizes a thin SiO_2 layer (either thermally grown or deposited), to mask the nitride. The SiO_2 layer is first etched using a resist mask, then the resist is stripped, and the patterned oxide serves as the etch mask for the nitride in the phosphoric acid etch. The Si_3N_4 etch rate is about 100 Å /min, but only 0-25Å /min for CVD SiO_2. Films of plasma-enhanced CVD Si_3N_4 have much higher etch rates than high temperature CVD Si_3N_4. The rates depend strongly on the film composition, which may be expressed as $Si_xN_yH_z$.

The added complexity of using an SiO_2 etch mask makes dry etching of Si_3N_4 an attractive alternative. In fact, the first widely used dry etch process for microelectronic applications was developed for etching Si_3N_4 for this reason (Fig. 15).

Wet Etching Aluminum

Wet etching of aluminum and aluminum alloy films is generally done in heated solutions (35-45°C) of phosphoric acid, nitric acid, acetic acid, and water[27]. A typical etch composition may be 80% phosphoric acid, 5 % nitric, 5% acetic and 10% water. The etch rate is in the range of 1000-3000 Å /min and depends on several factors including etchant composition and temperature, type of resist used, agitation of wafers during etch, and impurities or alloys in the predominantly aluminum film.

The chemical mechanism of wet etching aluminum proceeds as follows: The nitric acid forms aluminum oxide, and the phosphoric acid and water dissolve this material. Conversion to Al_2O_3 takes place simultaneously with the dissolution process.

One of the difficulties encountered in wet etching of aluminum is H_2 gas bubble evolution. These bubbles tend to adhere firmly, locally inhibiting etching. Mechanical agitation during etching, and the addition of agents which lower the interfacial tension, are used to minimize this problem. Periodic removal of the wafers from the etching solution also breaks the bubbles.

The H_2 bubble formation and other problems (e.g. local contamination of the developed

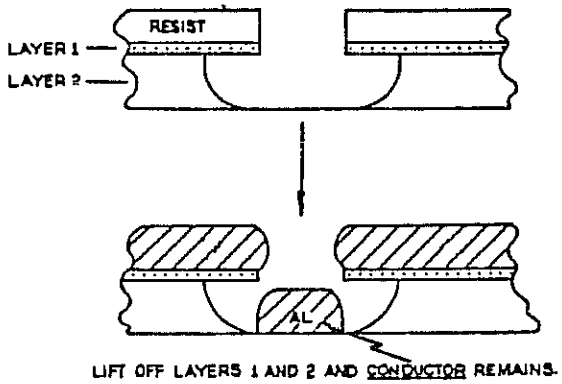

Fig. 16 Lift-off process for metallization.

metal, local oxidation, and delayed etching in certain locations [particularly in narrow spaces due to incomplete removal of resist residue]) delay the start of etching or prolong the time to clearly etch all the areas on the wafer. Thus, once the minimum etching time for a given pattern is established, 10-50% overetch time is usually added to assure the complete isolation of features.

LIFT-OFF TECHNOLOGY FOR PATTERNING

Lift-off is a technique for forming patterns on a wafer surface by an *additive process*, as opposed to the removal (or *subtractive*) process utilized in etching[28]. That is, in lift-off an inverse pattern is first formed in a so-called *stencil layer* present on the wafer, thereby exposing the substrate in specific locations (Fig. 16). Next the film to be patterned is deposited over the inverse-patterned stencil layer and the exposed substrate. Those portions which are deposited on the stencil layer are removed when the wafer is immersed in a liquid capable of dissolving the stencil layer. In other words, the depositied film on the stencil layer is *lifted-off* during the dissolution of the stencil. The film material that was deposited on the exposed substrate regions remains behind as the required pattern.

The key to a successful lift-off process is to insure that a distinct break exists between the film material on top of the stencil and that deposited on the exposed substrate. This separation allows the desolving liquid to reach and attack the stencil layer and also insures that the film atop the stencil is free to be lifted off. Cold evaporation over steep steps achieves such breaks. The major applications of lift-off techniques involve patterning of metals for interconnections.

The advantages of lift-off include the following: a) composite layers (e.g. Al / Ti / Al) can be sequentially deposited and then patterned with a *single* lift-off, as opposed to removal by multiple etch steps in an etching process; b) hard to remove residues, such as copper residues that are left when dry etching Al-Cu alloy films, are avoided since no etching of the patterned film is necessary; and c) the patterned film features can have sloped side walls, which makes them more easily covered by subsequent films (good step coverage).

On the other hand, although lift-off has received considerable attention because of the above advantages, it has several severe disadvantages which have made etching a far more popular patterning technology. These primarily involve difficulties in the creation of stencil layers that are compatible with the deposition, photolithographic, and dissolution processes that must also be successfully performed in order to create patterns by lift-off. We will list some of the lift-off processes as reported in the literature and describe in detail the process outlined by Fried, *et al*[32], for use in bipolar VLSI technology by IBM. The latter provides an example of the complexity

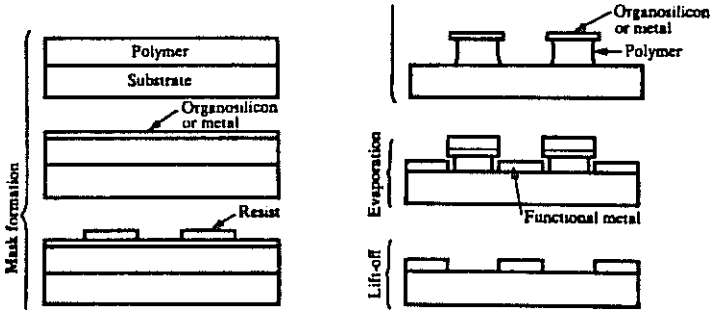

Fig. 17 Example of a lift-off sequence for bipolar VLSI circuits[32]. Copyright 1982 International Business Machines Corporation, reprinted with permission.

involved in fabricating suitable stencil layers.

Proposed stencil layers for lift-off have included: a) photoresist; b) two photoresist layers[29]; c) a photoresist / aluminum /photoresist layer[30]; d) polyimide /molybdenum layer; e) polyimide / polysulfone / SiO layer; f) inorganic dielectric layer /photoresist, as well as many others[31].

The lift-off process discussed by Fried[32] (Fig. 17) begins with the application of a thin polysulfone release layer onto a wafer, followed by a layer of positive photoresist (with a thickness exceeding that of the eventual metal layer). This composite structure is baked at a temperature of above 200°C in order to make it thermally stable at the elevated temperatures that will occur during subsequent metal deposition. Next a polysiloxane film (2000-3000Å thick) is spun on. Following another 200°C bake, the imaging photoresist is then applied. The imaging resist layer is now exposed and developed. A reactive-ion-etch step is used to reproduce the photoresist pattern into the polysiloxane, underlying resist and polysulfone layers. This step requires two sequential etch processes: one to etch the polysiloxane and the other for the remaining layers. The second etch also undercuts the polysiloxane and leaves an overhang that ensures that the deposited metal on the exposed substrate will be cleanly broken away from the metal deposited on top of the stencil. Upon completion of etching the stencil, any remaining imaging resist is stripped and the metal is evaporated. Lift-off is accomplished by immersing the wafers in N-methylpyrrolidone, which releases the polysulfone, and thereby also the resist, polysiloxane and the metal deposited thereon.

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PROBLEMS

1. If a layer is etched isotropically in a process in which neither the mask nor the substrate material is attacked by the etchant, sketch the profile of the etched feature at the instant when the layer is etched, and again after an overetch of 100% and 200% have been performed. What shape does the etched profile begin to assume as the overetch time is increased? From this data, if an etched feature is inspected after stripping the resist and vertical walls are observed, can it be concluded that the etch process has been achieved in an anisotropic manner?
2. Why has ammonium persulfate been recommended as a replacement for sulfuric acid in inorganic resist-stripping solutions?
3. Explain how faceting, sputtering from the backing plate, gas phase collisions, and collisions with shutters or cathode surfaces can cause contamination during *in situ* sputter etch cleaning steps.
4. Show that Eq. 11 is the valid expression for the uniformity factor when the worst-case condition of *the thinnest and fastest etching portion of a film is assumed to lie over the fastest*

etching region of the substrate.

5. A window in SiO_2 which is 5000Å thick is to be etched over a region of Si substrate containing a 2500Å deep pn junction. It is decided that no more than 1500Å of this junction thickness can be removed during the etch. Determine the S_{fs} if the oxide thickness uniformity is ±5%, the etch rate uniformity is ±10%, and a 20% overetch is specified.

6. Polysilicon features 4000Å thick cross over a field oxide step of 7000Å in height and over a gate SiO_2 layer that is 300Å thick. Determine the S_{fm} and S_{fs} if the polysilicon etch rate uniformity is ±5 %, and A = 1 and A_m = 0.4. In this problem the polysilicon thickness uniformity is ±3%, the mask edge profile is 80°, it is desired to control the linewidth to 0.1 μm, and the mask etch rate uniformity is ±3%.

7. Explain how the isoetch curves of Fig. 13 are interpreted. If silicon is to be etched in a solution of HF: HNO_3: CH_3COOH = 1:x:1, show how the etch rate changes as x is varied from 1 to 20.

8. Describe some of the problems associated with wet etching of aluminum.

9. Summarize the advantages and prolems of lift-off as a patterning technique.

10. Suggest some problems that may be encountered when resist is stripped by dry-etching.